

P398_A02: G92-600/700/975, G3-256, MXM V2.0, MXM-III
LVDS, DVI-D, HDMI, VIDEO OUT, VGA, HDCP, SLI
8/16/32Mx32 GDDR3, 256Bit, 256/512/1024MB

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SKU	VARIANT	NVPN	ASSEMBLY
8	BASE	600-10398-BASE-200	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10398-0001-200	NB8E-GT/G92-700, 512MB, 8pcs 16Mx32 GDDR3
2	SKU0003	600-10398-0003-200	NB8E-GTX/G92-720, 512MB, 8pcs 16Mx32 GDDR3
3	SKU0500	600-50398-0500-200	WS SKU NB8E-GLM3/G92-975, with HDCP kit, 512MB, 8pcs 16Mx32 GDDR3 for blade application
4	SKU0501	600-50398-0501-200	WS SKU NB8E-GLM3/G92-975, with HDCP kit, 512MB, 8pcs 16Mx32 GDDR3
5	SKU0006	600-10398-0006-200	MXM-III NB8E-GT/G92-700, 512MB, 8pcs 16Mx32 GDDR3 for APPLE
6	SKU0502	600-50398-0502-200	WS MOBILE, G92-985, 512MB, HP Absolut
7	SKU0503	600-50398-0503-200	WS MOBILE, G92-985, 1GB, HP Absolut
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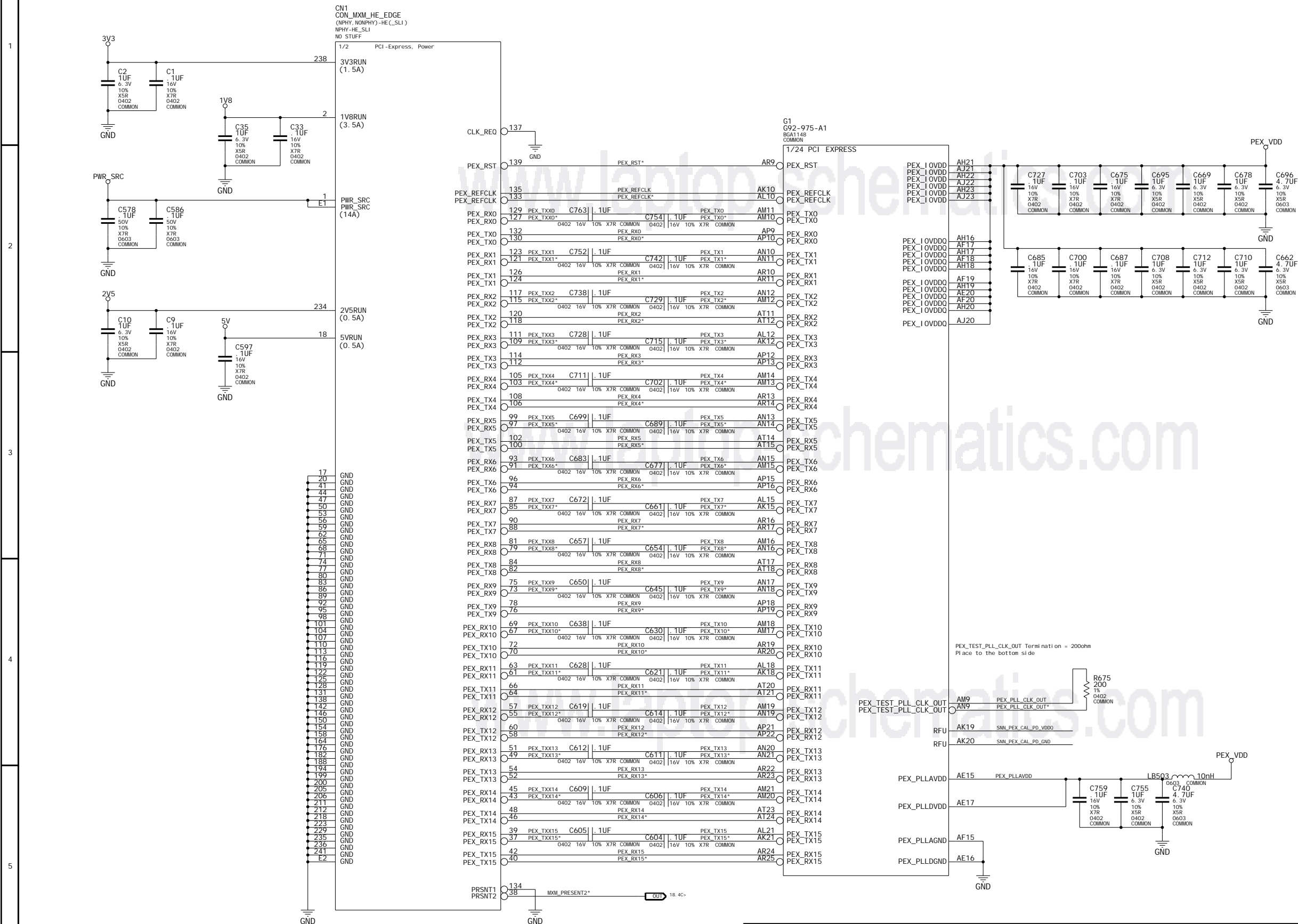
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Page2: MXM-III and PCI-EX Connector



POWER NET RULES

	NET	VOLTAGE	MAX_CURRENT	MIN_LINE_WIDTH
	PEX_PLLAVDD	1.2V	0.25A	16MIL

PLATFORM POWER NET RULES

	NET	VOLTAGE	NV_MAX_MAX_ CURRENT	MIN_L1_LINE_ WIDTH	NV_SOURCE_ POWER_NET
PWR_SRC	PWR_SRC	20V	16A	16MI L	TRUE
5V	5V	5V	0.5A	16MI L	TRUE
3V3	3V3	3.3V	1.5A	16MI L	TRUE
2V5	2V5	2.5V	0.5A	16MI L	TRUE
1V8	1V8	1.8V	3.5A	16MI L	TRUE
	GND			20MI L	

NET RULES

NET	NV_CRITICAL_NET	DIFFPAIR	NV_IMPEDANCE
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B1	PEX_PLL_CLK_OUT			
B1	PEX_PLL_CLK_OUT*			
B1	PEX_REFCLK*	1	PEX_REFCLK	1000 MHz
B1	PEX_REFCLK*	1	PEX_REFCLK	1000 MHz
B1	PEX_TX0	1	PEX_TX0	1000 MHz
B1	PEX_TX0*	1	PEX_TX0	1000 MHz
B1	PEX_TX1	1	PEX_TX1	1000 MHz
B1	PEX_TX1*	1	PEX_TX1	1000 MHz
B1	PEX_TX2	1	PEX_TX2	1000 MHz
B1	PEX_TX2*	1	PEX_TX2	1000 MHz
B1	PEX_TX3	1	PEX_TX3	1000 MHz
B1	PEX_TX3*	1	PEX_TX3	1000 MHz
B1	PEX_TX4	1	PEX_TX4	1000 MHz
B1	PEX_TX4*	1	PEX_TX4	1000 MHz
B1	PEX_TX5	1	PEX_TX5	1000 MHz
B1	PEX_TX5*	1	PEX_TX5	1000 MHz
B1	PEX_TX6	1	PEX_TX6	1000 MHz
B1	PEX_TX6*	1	PEX_TX6	1000 MHz
B1	PEX_TX7	1	PEX_TX7	1000 MHz
B1	PEX_TX7*	1	PEX_TX7	1000 MHz
B1	PEX_TX8	1	PEX_TX8	1000 MHz
B1	PEX_TX8*	1	PEX_TX8	1000 MHz
B1	PEX_TX9	1	PEX_TX9	1000 MHz
B1	PEX_TX9*	1	PEX_TX9	1000 MHz
B1	PEX_TX10	1	PEX_TX10	1000 MHz
B1	PEX_TX10*	1	PEX_TX10	1000 MHz
B1	PEX_TX11	1	PEX_TX11	1000 MHz
B1	PEX_TX11*	1	PEX_TX11	1000 MHz
B1	PEX_TX12	1	PEX_TX12	1000 MHz
B1	PEX_TX12*	1	PEX_TX12	1000 MHz
B1	PEX_TX13	1	PEX_TX13	1000 MHz
B1	PEX_TX13*	1	PEX_TX13	1000 MHz
B1	PEX_TX14	1	PEX_TX14	1000 MHz
B1	PEX_TX14*	1	PEX_TX14	1000 MHz
B1	PEX_TX15	1	PEX_TX15	1000 MHz
B1	PEX_TX15*	1	PEX_TX15	1000 MHz

B1	PEX_TX00	1	PEX_TX00	1000H
B1	PEX_TX00*	1	PEX_TX00	1000H
B1	PEX_TX01	1	PEX_TX01	1000H
B1	PEX_TX01*	1	PEX_TX01	1000H
B1	PEX_TX02	1	PEX_TX02	1000H
B1	PEX_TX02*	1	PEX_TX02	1000H
B1	PEX_TX03	1	PEX_TX03	1000H
B1	PEX_TX03*	1	PEX_TX03	1000H
B1	PEX_TX04	1	PEX_TX04	1000H
B1	PEX_TX04*	1	PEX_TX04	1000H
B1	PEX_TX05	1	PEX_TX05	1000H
B1	PEX_TX05*	1	PEX_TX05	1000H
B1	PEX_TX06	1	PEX_TX06	1000H
B1	PEX_TX06*	1	PEX_TX06	1000H
B1	PEX_TX07	1	PEX_TX07	1000H
B1	PEX_TX07*	1	PEX_TX07	1000H
B1	PEX_TX08	1	PEX_TX08	1000H
B1	PEX_TX08*	1	PEX_TX08	1000H
B1	PEX_TX09	1	PEX_TX09	1000H
B1	PEX_TX09*	1	PEX_TX09	1000H
B1	PEX_TX010	1	PEX_TX010	1000H
B1	PEX_TX010*	1	PEX_TX010	1000H
B1	PEX_TX011	1	PEX_TX011	1000H
B1	PEX_TX011*	1	PEX_TX011	1000H
B1	PEX_TX012	1	PEX_TX012	1000H
B1	PEX_TX012*	1	PEX_TX012	1000H
B1	PEX_TX013	1	PEX_TX013	1000H
B1	PEX_TX013*	1	PEX_TX013	1000H
B1	PEX_TX014	1	PEX_TX014	1000H
B1	PEX_TX014*	1	PEX_TX014	1000H
B1	PEX_TX015	1	PEX_TX015	1000H
B1	PEX_TX015*	1	PEX_TX015	1000H

	PEX_R0	1	PEX_R0	10001
B1	PEX_R0*	1	PEX_R0	10001
B1	PEX_R01	1	PEX_R01	10001
B1	PEX_R01*	1	PEX_R01	10001
B1	PEX_R02	1	PEX_R02	10001
B1	PEX_R02*	1	PEX_R02	10001
B1	PEX_R03	1	PEX_R03	10001
B1	PEX_R03*	1	PEX_R03	10001
B1	PEX_R04	1	PEX_R04	10001
B1	PEX_R04*	1	PEX_R04	10001
B1	PEX_R05	1	PEX_R05	10001
B1	PEX_R05*	1	PEX_R05	10001
B1	PEX_R06	1	PEX_R06	10001
B1	PEX_R06*	1	PEX_R06	10001
B1	PEX_R07	1	PEX_R07	10001
B1	PEX_R07*	1	PEX_R07	10001
B1	PEX_R08	1	PEX_R08	10001
B1	PEX_R08*	1	PEX_R08	10001
B1	PEX_R09	1	PEX_R09	10001
B1	PEX_R09*	1	PEX_R09	10001
B1	PEX_R010	1	PEX_R010	10001
B1	PEX_R010*	1	PEX_R010	10001
B1	PEX_R011	1	PEX_R011	10001
B1	PEX_R011*	1	PEX_R011	10001
B1	PEX_R012	1	PEX_R012	10001
B1	PEX_R012*	1	PEX_R012	10001
B1	PEX_R013	1	PEX_R013	10001
B1	PEX_R013*	1	PEX_R013	10001
B1	PEX_R014	1	PEX_R014	10001
B1	PEX_R014*	1	PEX_R014	10001
B1	PEX_R015	1	PEX_R015	10001
B1	PEX_R015*	1	PEX_R015	10001

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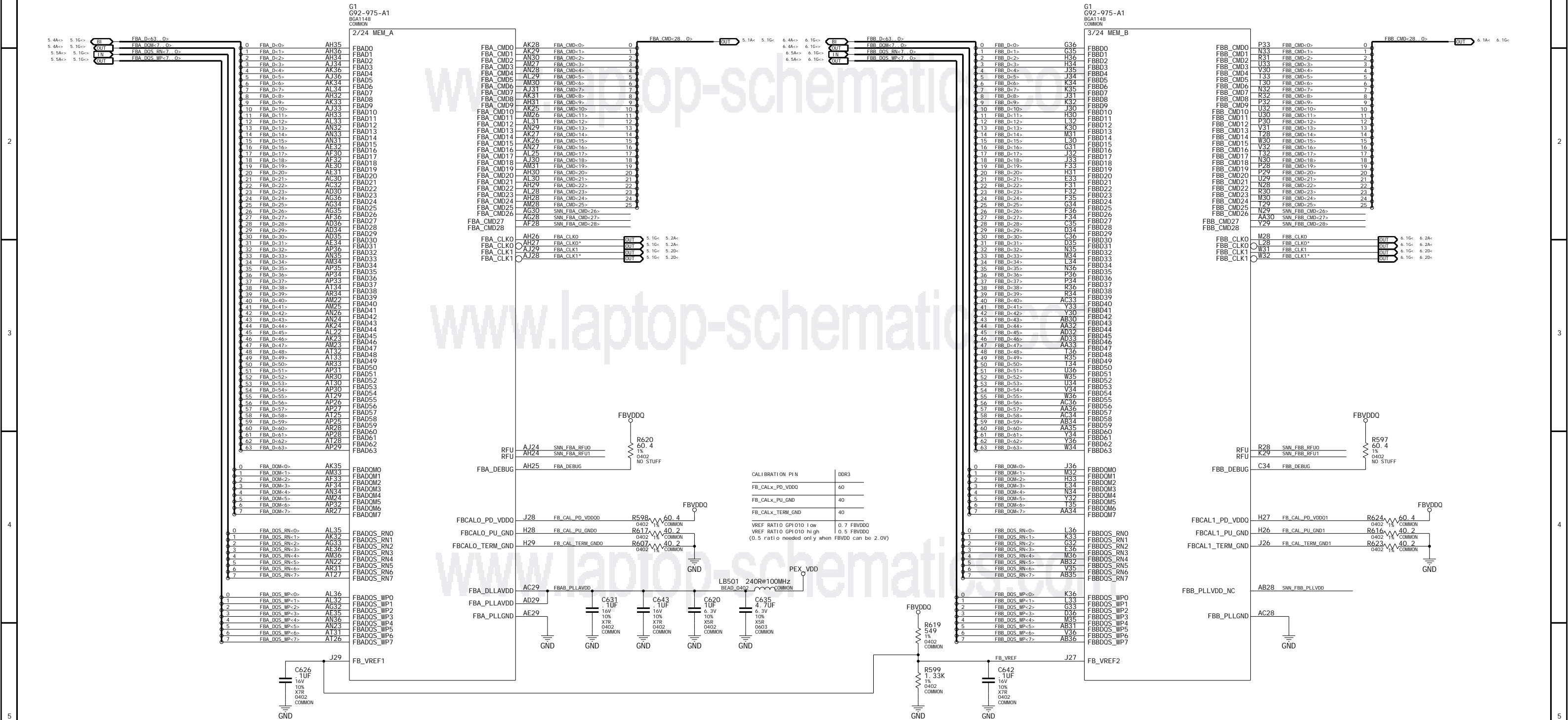
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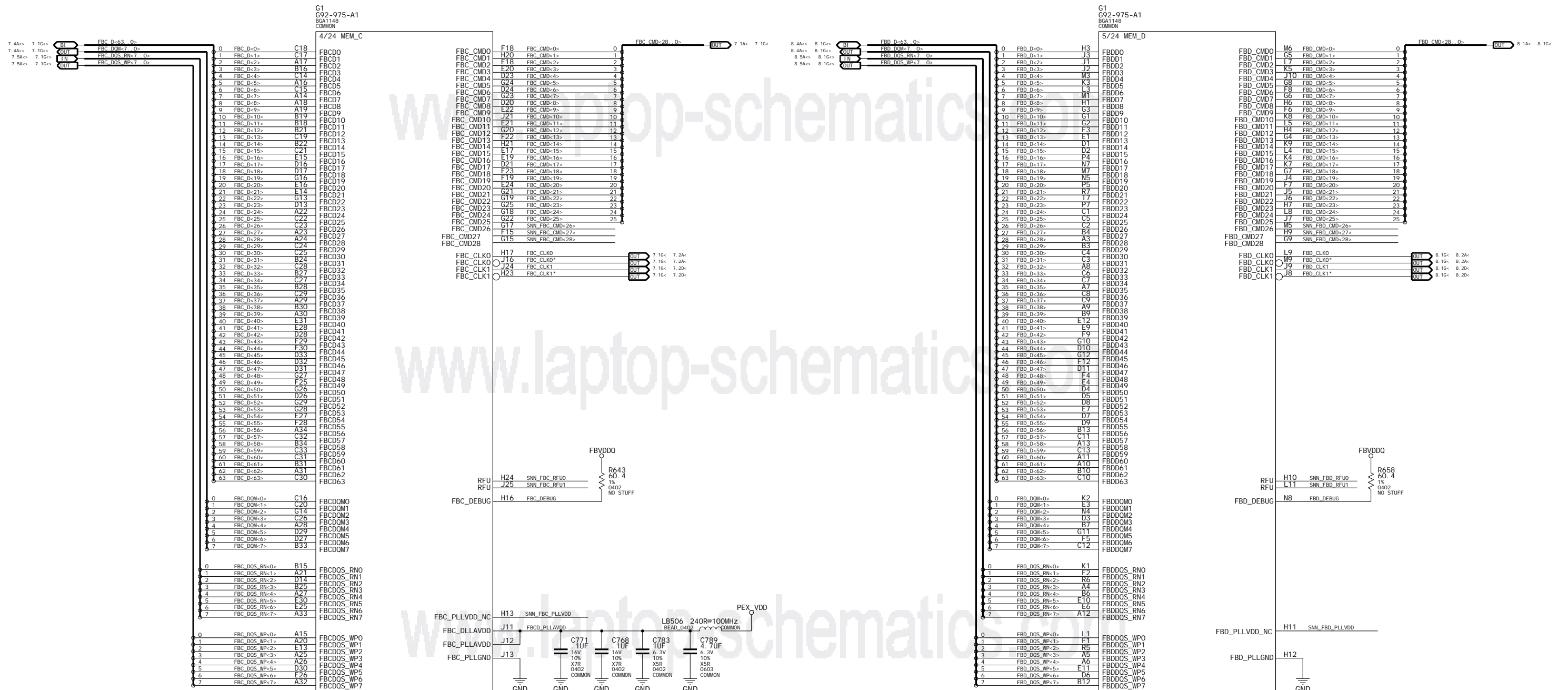
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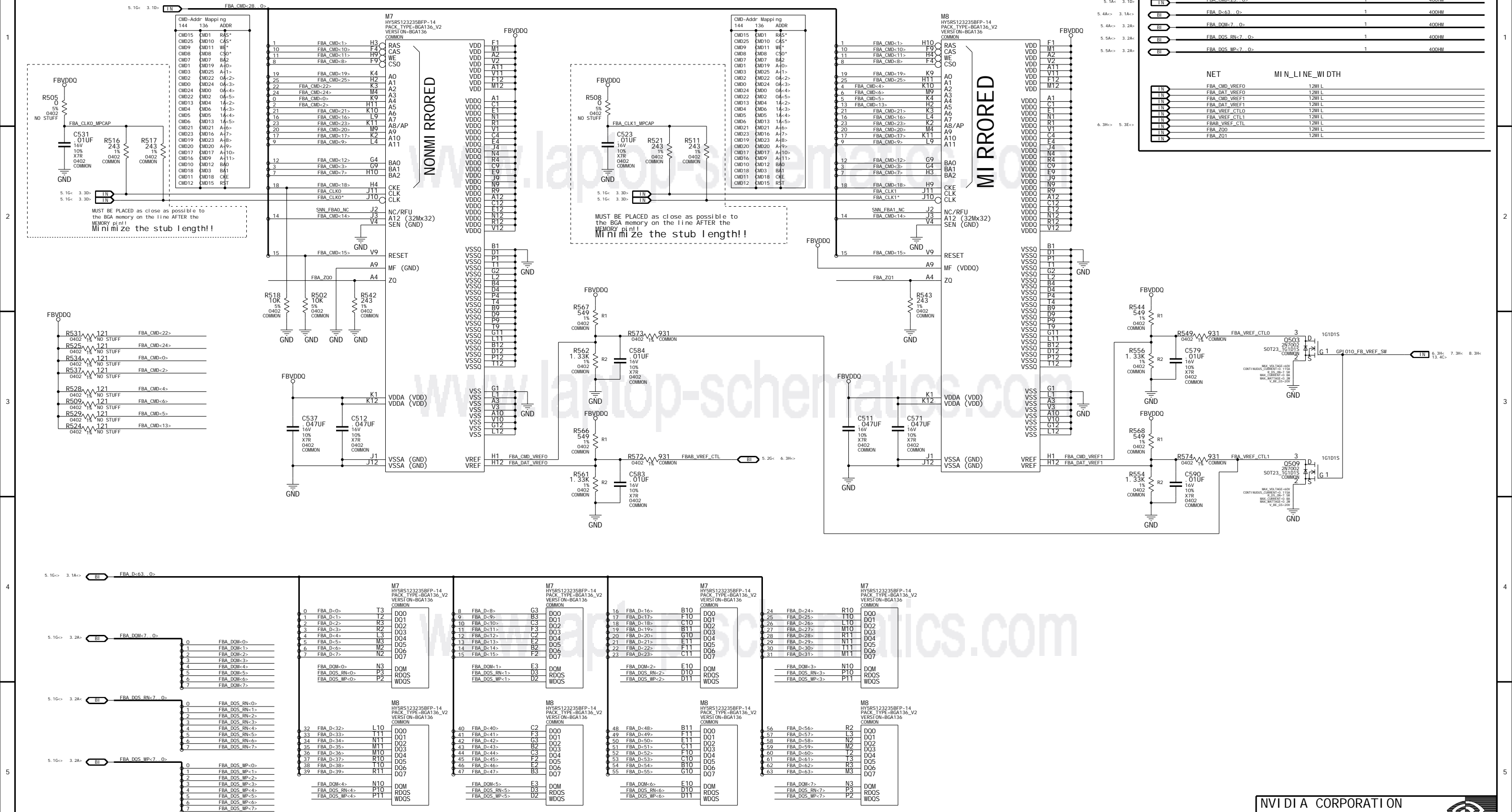
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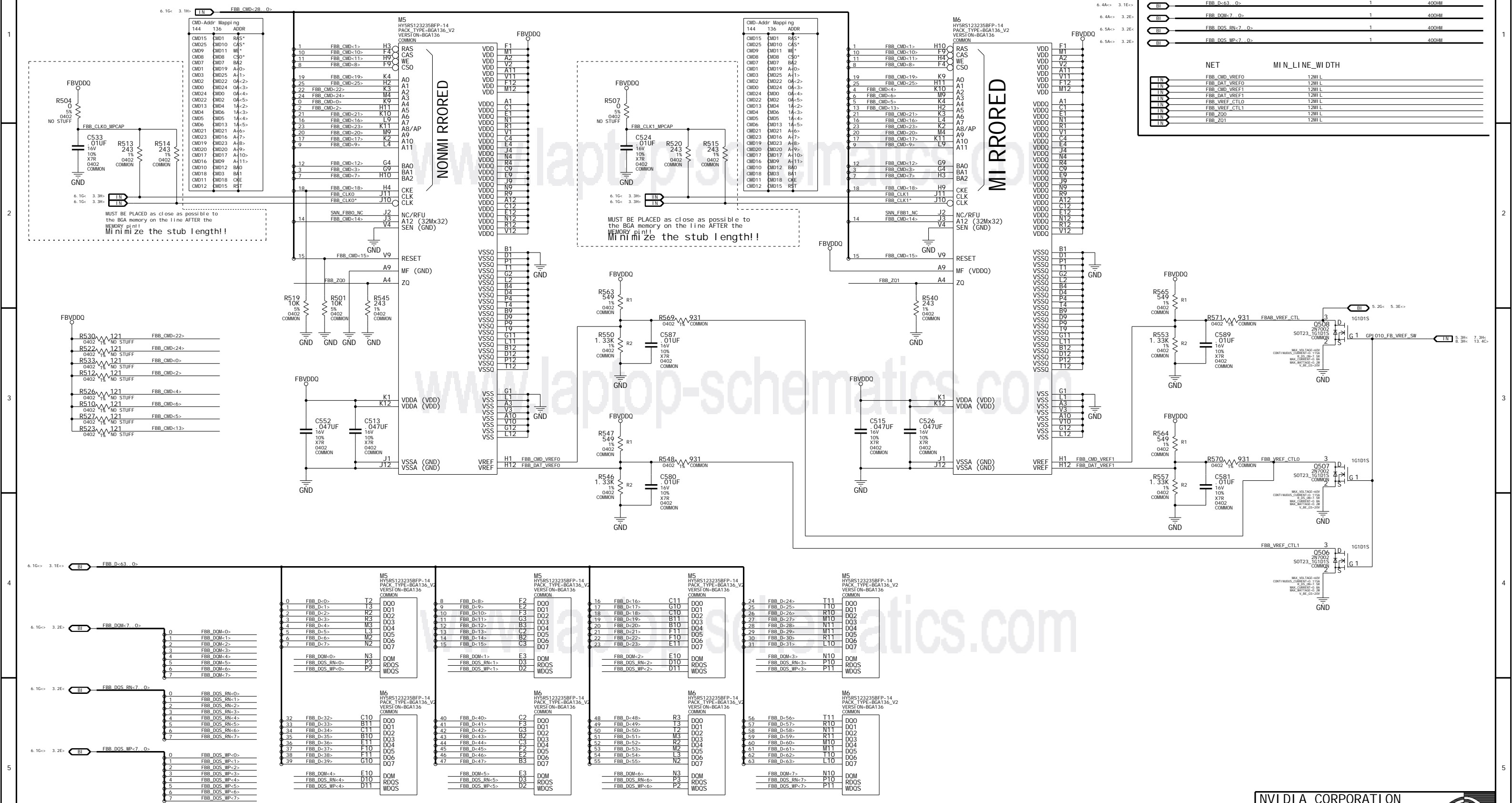
	NET	VOLTAGE	MAX_CURRENT	MIN_L1_NE_WIDTH
	FBAB_PL_LAVDD	1.2V	0.25A	16MI L
	FB_VREF			12MI L
	FB_CAL_PD_VDD00			12MI L
	FB_CAL_PU_GND0			12MI L
	FB_CAL_TERM_GND0			12MI L
	FB_CAL_PD_VDD01			12MI L
	FB_CAL_PU_GND1			12MI L
	FB_CAL_TERM_GND1			12MI L
	NET	NV_CRI TI CAL		NV_I IMPEDANCE
	FBA_DEBUG	1		400HM
	FBF_DEBUG	1		400HM

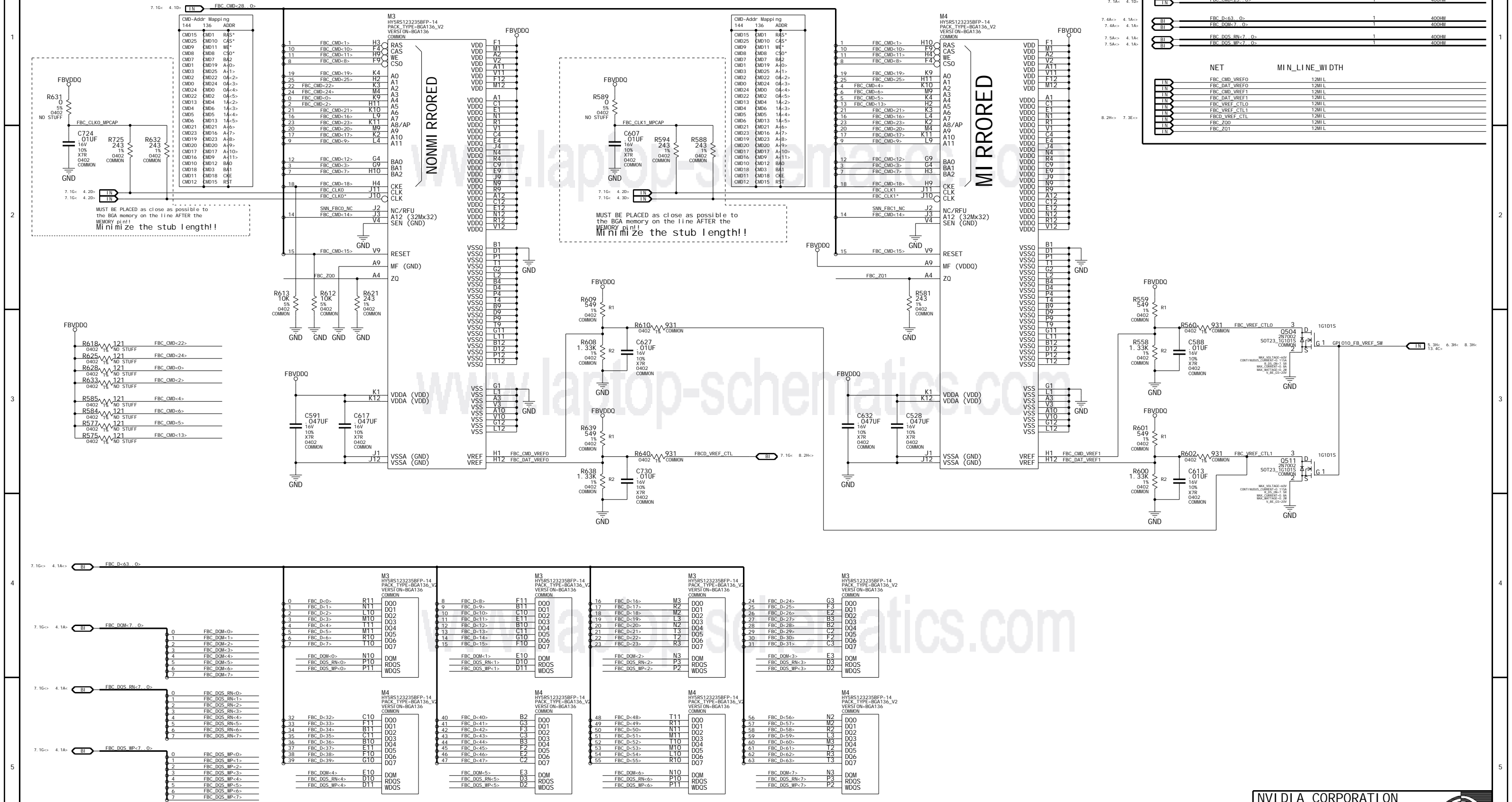


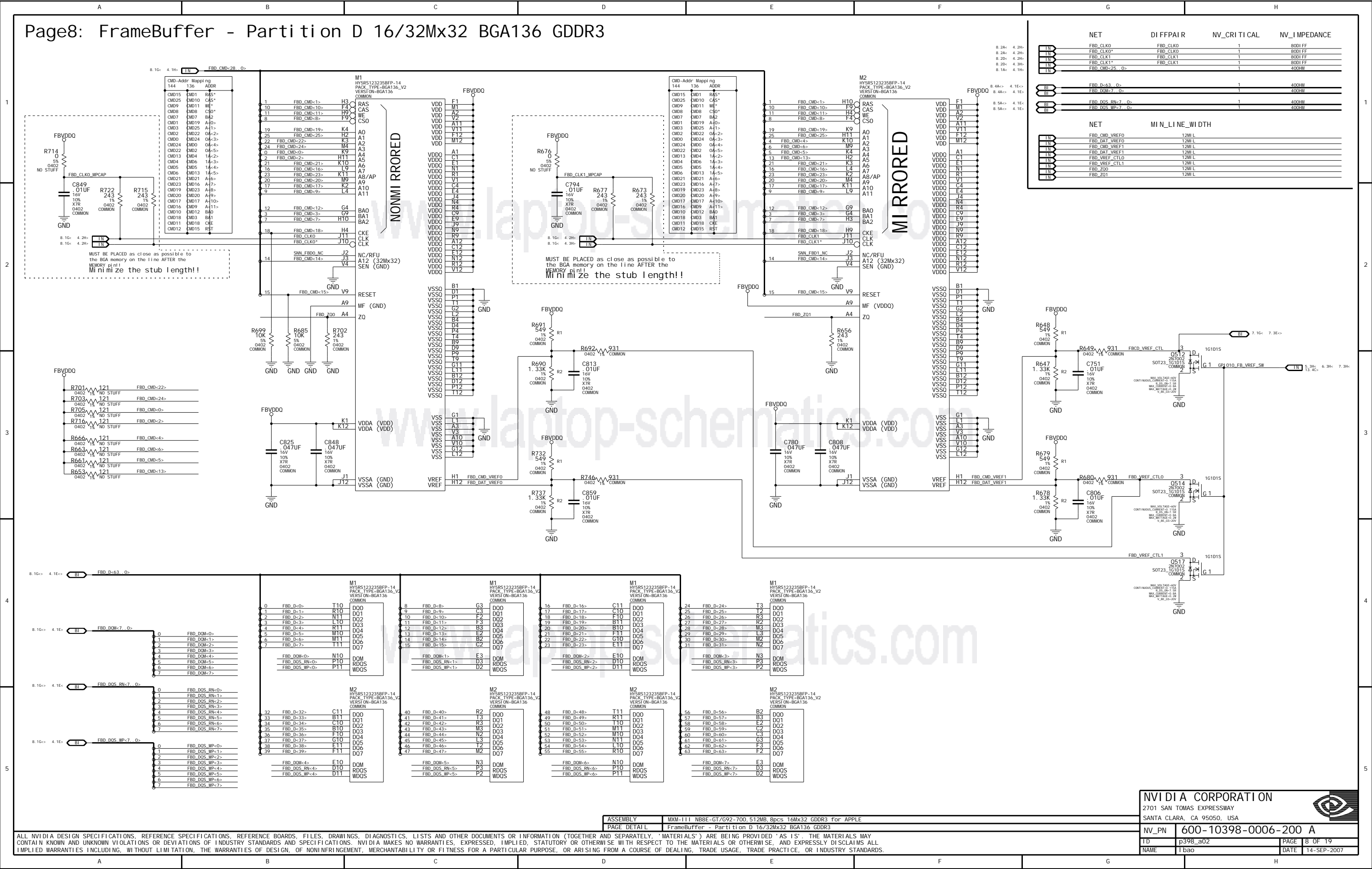
	NET	VOLTAGE	MAX_CURRENT	MIN_LENGTH_WIDTH
1	FBCD_PL_LAVDD	1.2V	0.25A	16mil
	NET	NV_CRI_T1_CAL	NV_IIMPEDANCE	
1	FBC_DEBUG	1	400HM	
1	FBD_DEBUG	1	400HM	



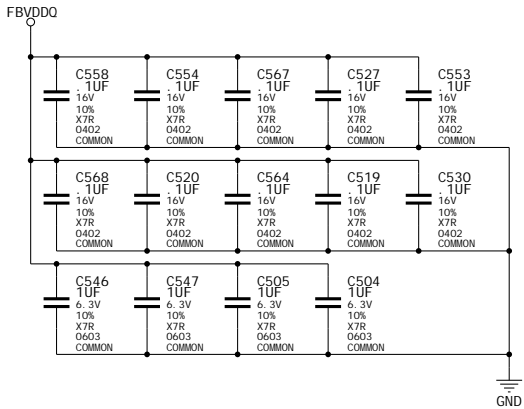




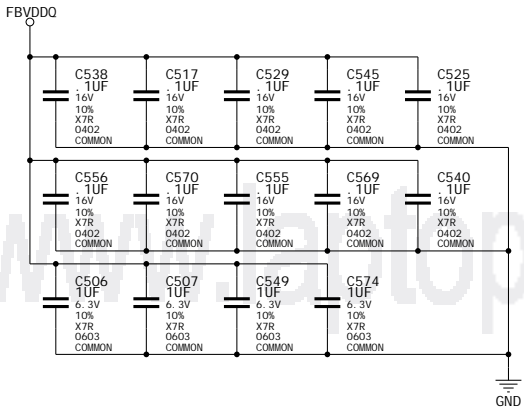




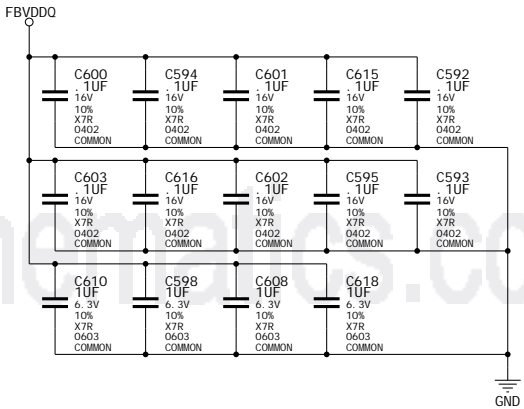
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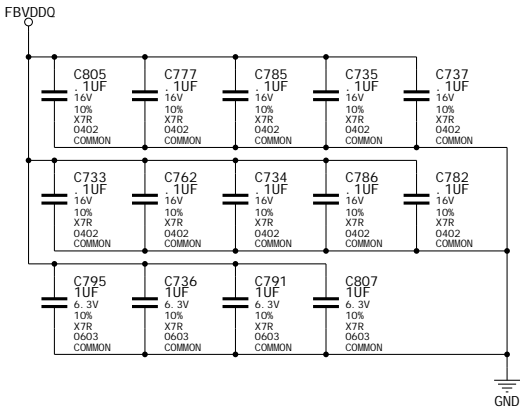
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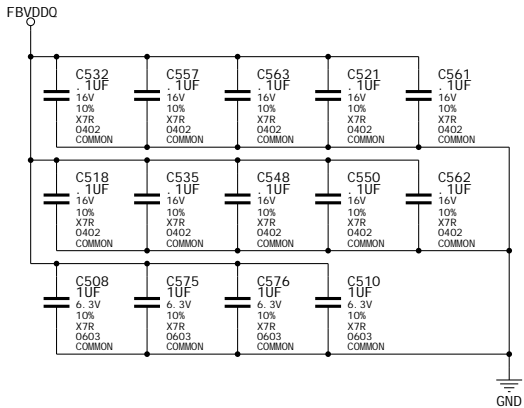
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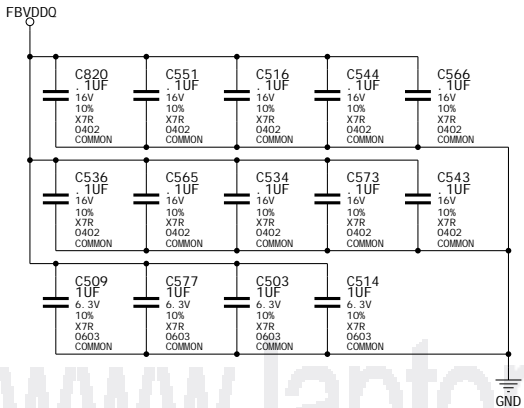
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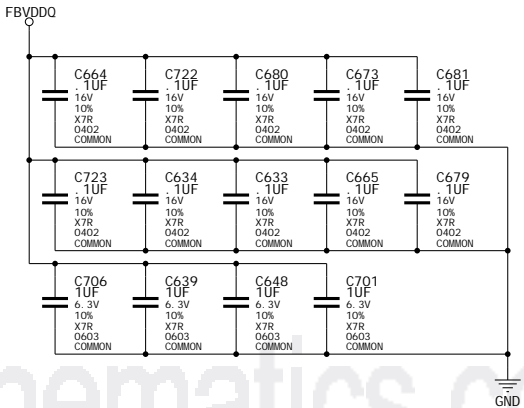
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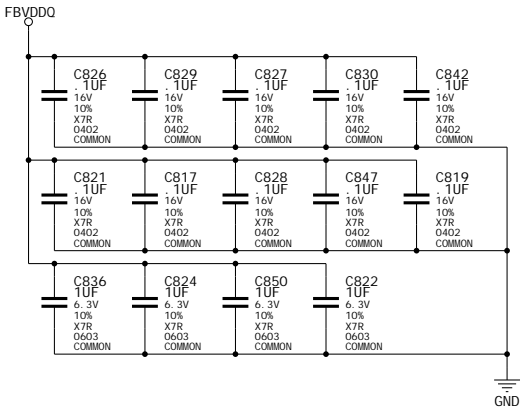
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FBC - bottom



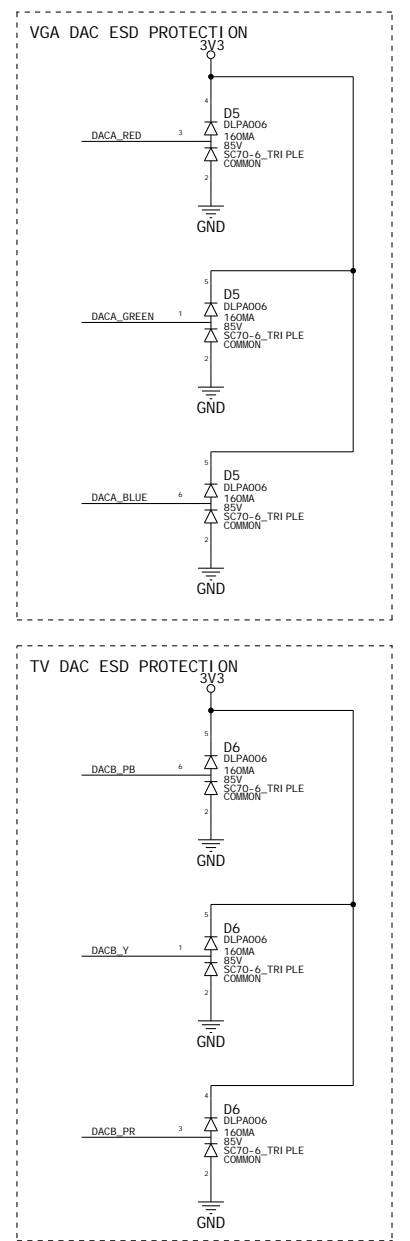
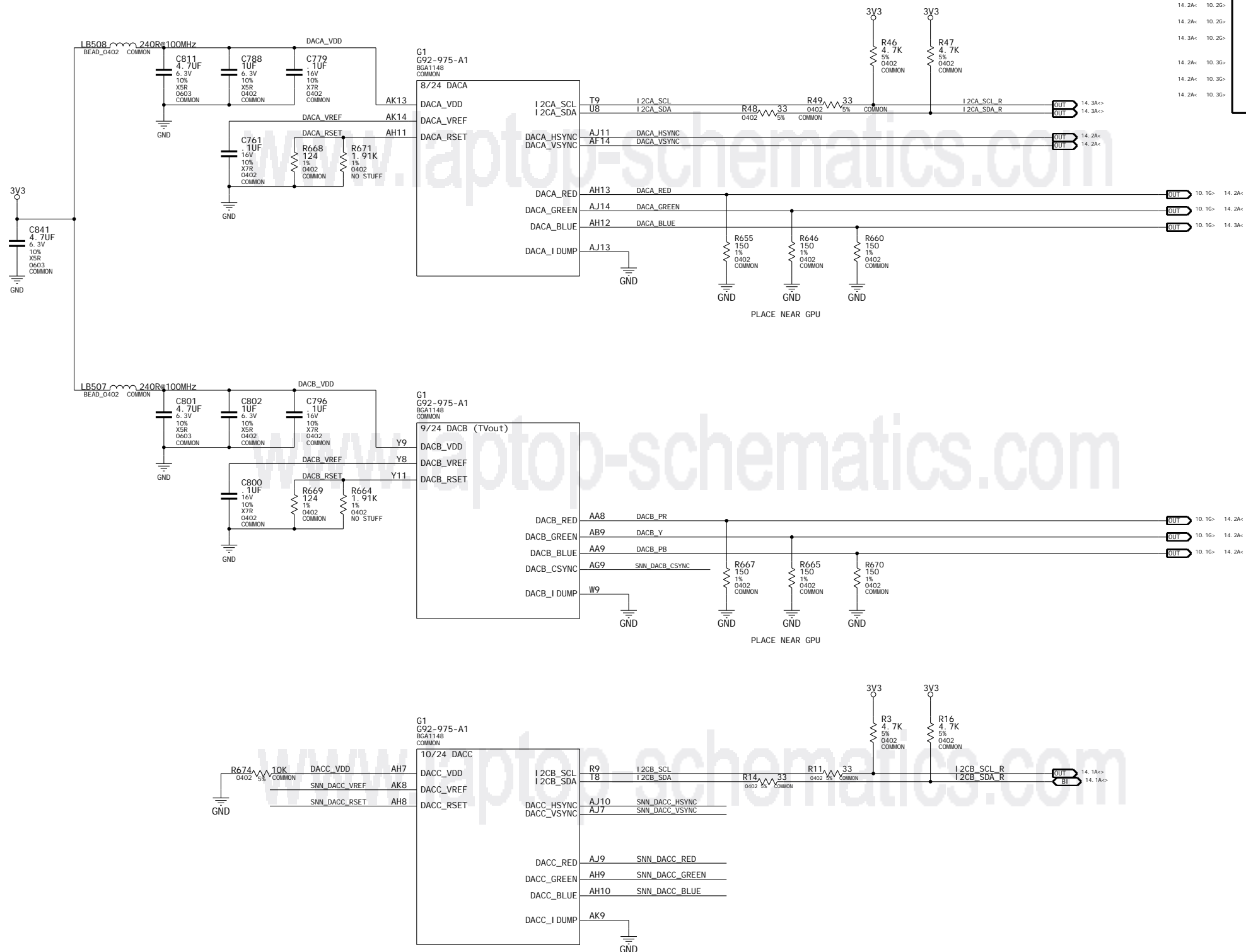
FBD - bottom



Page10: DACA, DACB, and DACC Interface

NET	VOLTAGE	MAX_CURRENT	MIN_LINE_WIDTH
1N DACA_VDD	3.3V	0.35A	16MIL
1N DACB_VDD	3.3V	0.35A	16MIL
1N DACA_VDD			12MIL
1N DACA_VREF			12MIL
1N DACA_RSET			12MIL
1N DACB_VREF			12MIL
1N DACB_RSET			12MIL

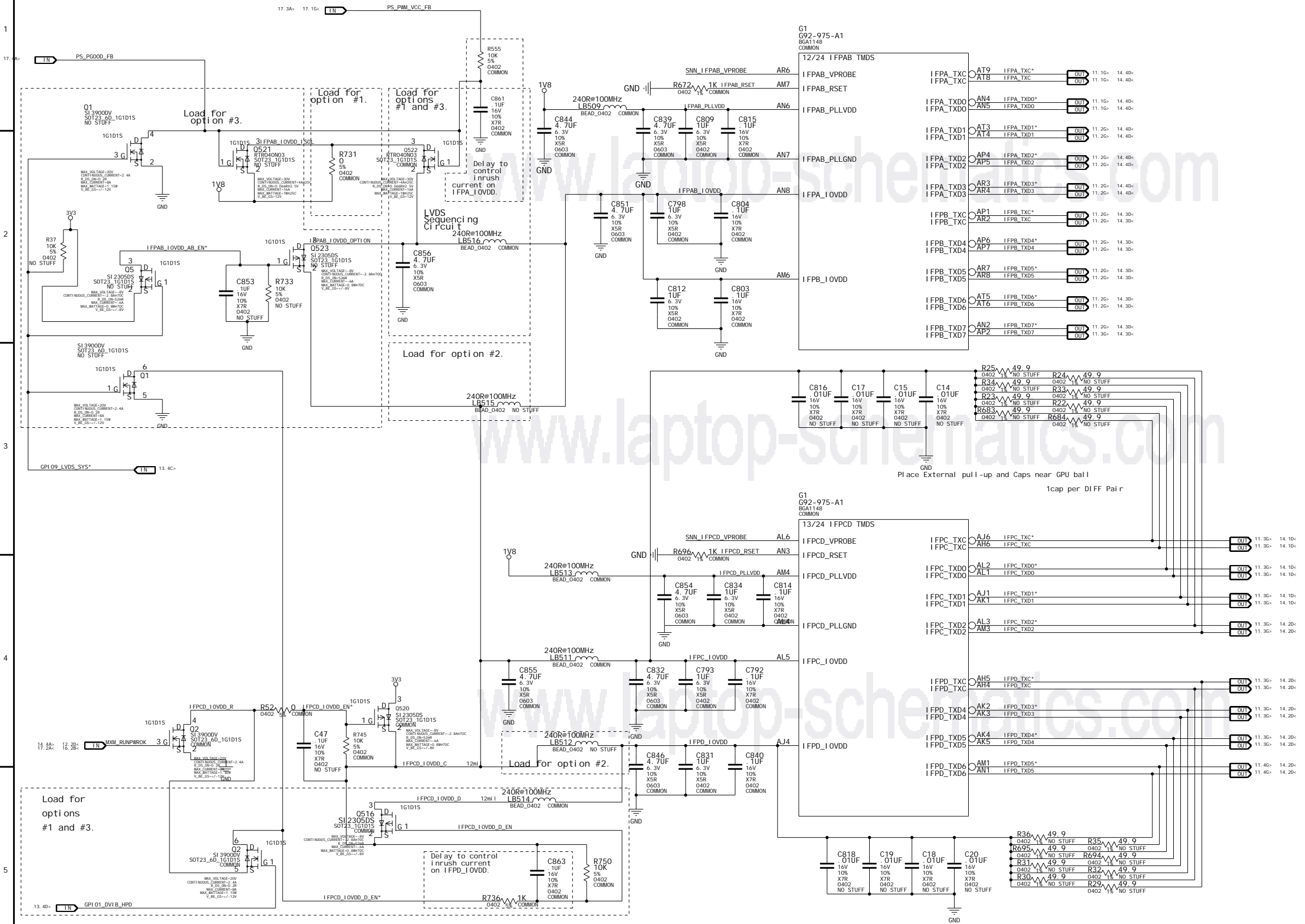
NET	NV_IMPEDANCE	NV_Critical_NET
OUT1 DACA_RED	500HM	1
OUT1 DACA_GREEN	500HM	1
OUT1 DACA_BLUE	500HM	1
OUT1 DACB_PR	500HM	1
OUT1 DACB_Y	500HM	1
OUT1 DACB_PB	500HM	1



Page11: IFPA/B LVDS Output and IFPC/D TMD5 Output

Loading options for IFPA/B outputs

- Option #1) IFPA/B outputs to LVDS only.
Option #2) IFPA/B outputs to DVI-C only.
Option #3) Controlled with GPI09, IFPA/B dynamically outputs to LVDS or DVI-C.



NET	VOLTAGE	MAX_CURRENT	MIN_LINE_WIDTH
IFPA_B_PLLVDD	1.8V	0.20A	16MIL
IFPA_B_I0VDD	3.3V	0.40A	16MIL
IFPC_I0VDD	3.3V	0.20A	16MIL
IFPD_I0VDD	3.3V	0.20A	16MIL
IFPCD_PLLVDD	1.8V	0.20A	16MIL
IFPA_B_RSET			12MIL
IFPCD_RSET			12MIL

NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPA_TXC*	IFPA_TXC	1	100DI FF
IFPA_TXC	IFPA_TXC	1	100DI FF
IFPA_TXD0*	IFPA_TXD0	1	100DI FF
IFPA_TXD0	IFPA_TXD0	1	100DI FF
IFPA_TXD1*	IFPA_TXD1	1	100DI FF
IFPA_TXD1	IFPA_TXD1	1	100DI FF
IFPA_TXD2*	IFPA_TXD2	1	100DI FF
IFPA_TXD2	IFPA_TXD2	1	100DI FF
IFPA_TXD3*	IFPA_TXD3	1	100DI FF
IFPA_TXD3	IFPA_TXD3	1	100DI FF
IFPB_TXC*	IFPB_TXC	1	100DI FF
IFPB_TXC	IFPB_TXC	1	100DI FF
IFPB_TXD4*	IFPB_TXD4	1	100DI FF
IFPB_TXD4	IFPB_TXD4	1	100DI FF
IFPB_TXD5*	IFPB_TXD5	1	100DI FF
IFPB_TXD5	IFPB_TXD5	1	100DI FF
IFPB_TXD6*	IFPB_TXD6	1	100DI FF
IFPB_TXD6	IFPB_TXD6	1	100DI FF
IFPB_TXD7*	IFPB_TXD7	1	100DI FF
IFPB_TXD7	IFPB_TXD7	1	100DI FF
IFPC_TXC*	IFPC_TXC	1	100DI FF
IFPC_TXC	IFPC_TXC	1	100DI FF
IFPC_TXD0*	IFPC_TXD0	1	100DI FF
IFPC_TXD0	IFPC_TXD0	1	100DI FF
IFPC_TXD1*	IFPC_TXD1	1	100DI FF
IFPC_TXD1	IFPC_TXD1	1	100DI FF
IFPC_TXD2*	IFPC_TXD2	1	100DI FF
IFPC_TXD2	IFPC_TXD2	1	100DI FF
IFPD_TXC*	IFPD_TXC	1	100DI FF
IFPD_TXC	IFPD_TXC	1	100DI FF
IFPD_TXD3*	IFPD_TXD3	1	100DI FF
IFPD_TXD3	IFPD_TXD3	1	100DI FF
IFPD_TXD4*	IFPD_TXD4	1	100DI FF
IFPD_TXD4	IFPD_TXD4	1	100DI FF
IFPD_TXD5*	IFPD_TXD5	1	100DI FF
IFPD_TXD5	IFPD_TXD5	1	100DI FF

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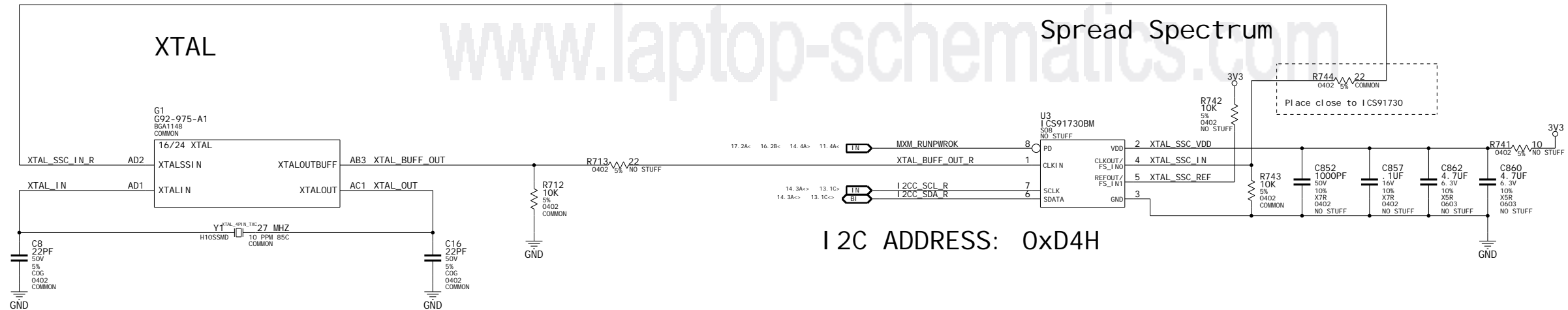


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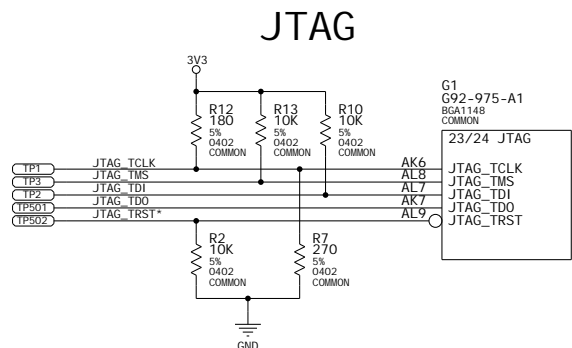
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NET		VOLTAGE	MIN LINE WIDTH
IN	XTAL_SSC_VDD	3.3V	16MIL
IN	XTAL_SSC_REF		12MIL

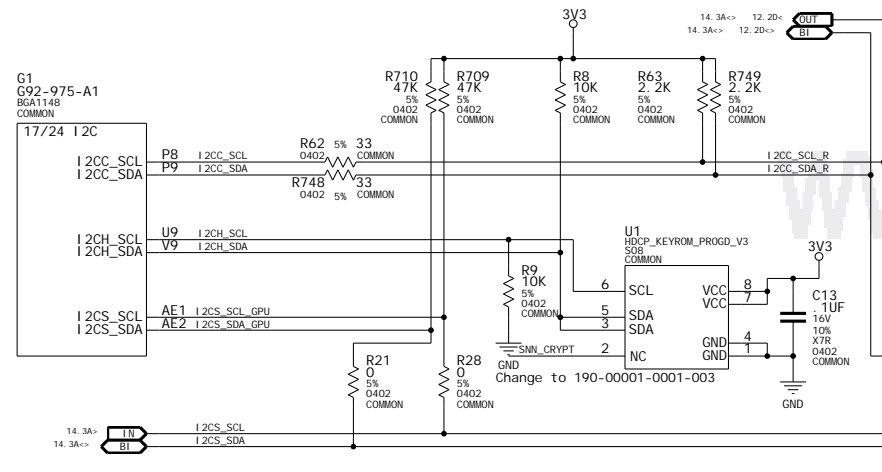
NET	NV_I MPEDANCE	NV_CRI TICAL_NET
OUT	XTAL_IN	50OHM
OUT	XTAL_OUT	50OHM
OUT	XTAL_BUFF_OUT	50OHM
OUT	XTAL_BUFF_OUT_R	50OHM
OUT	XTAL_SSC_IN	50OHM
OUT	XTAL_SSC_IN_R	50OHM



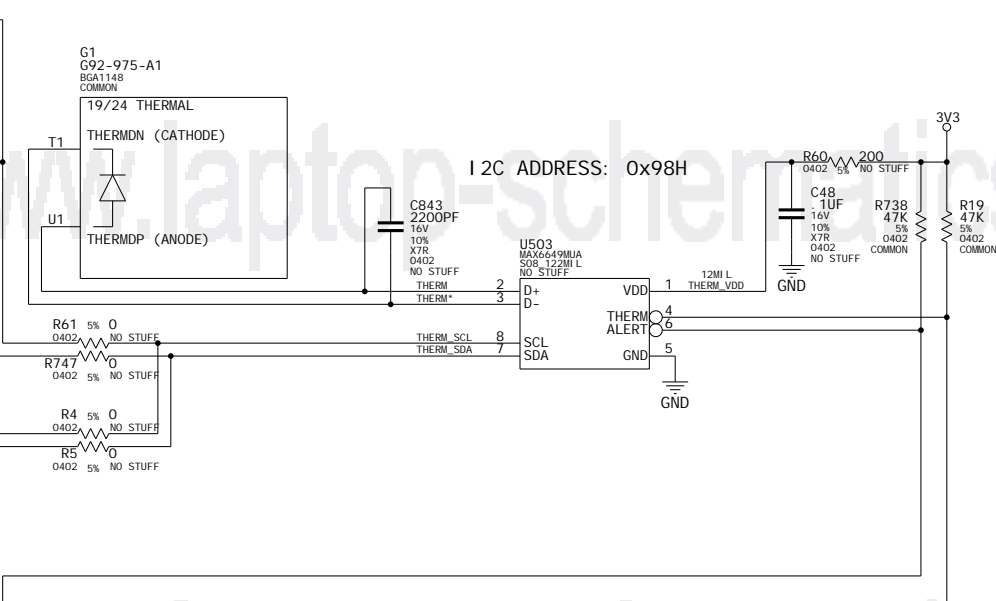
I 2C ADDRESS: 0xD4H



HDCP ROM



THERMAL DIODE

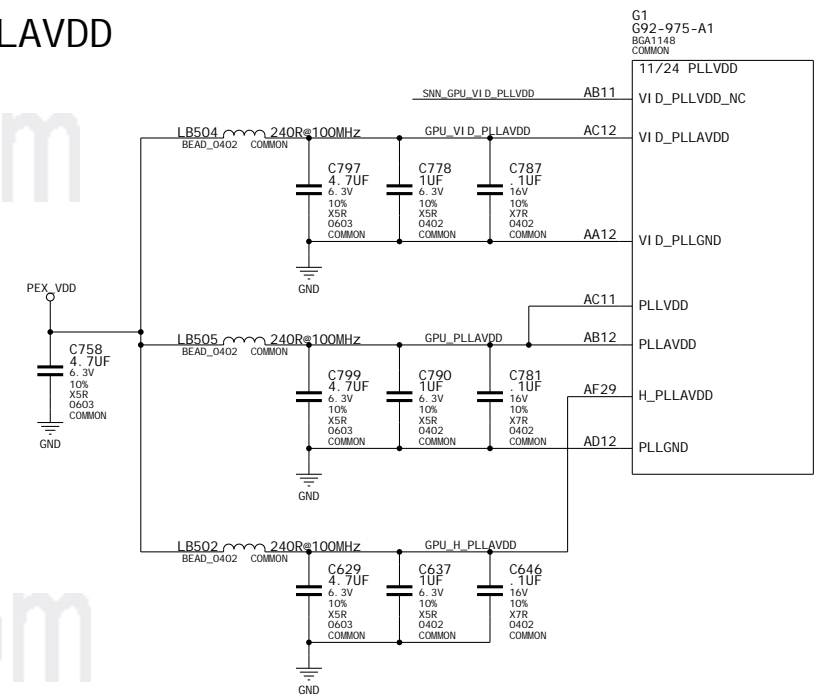


NET RULES

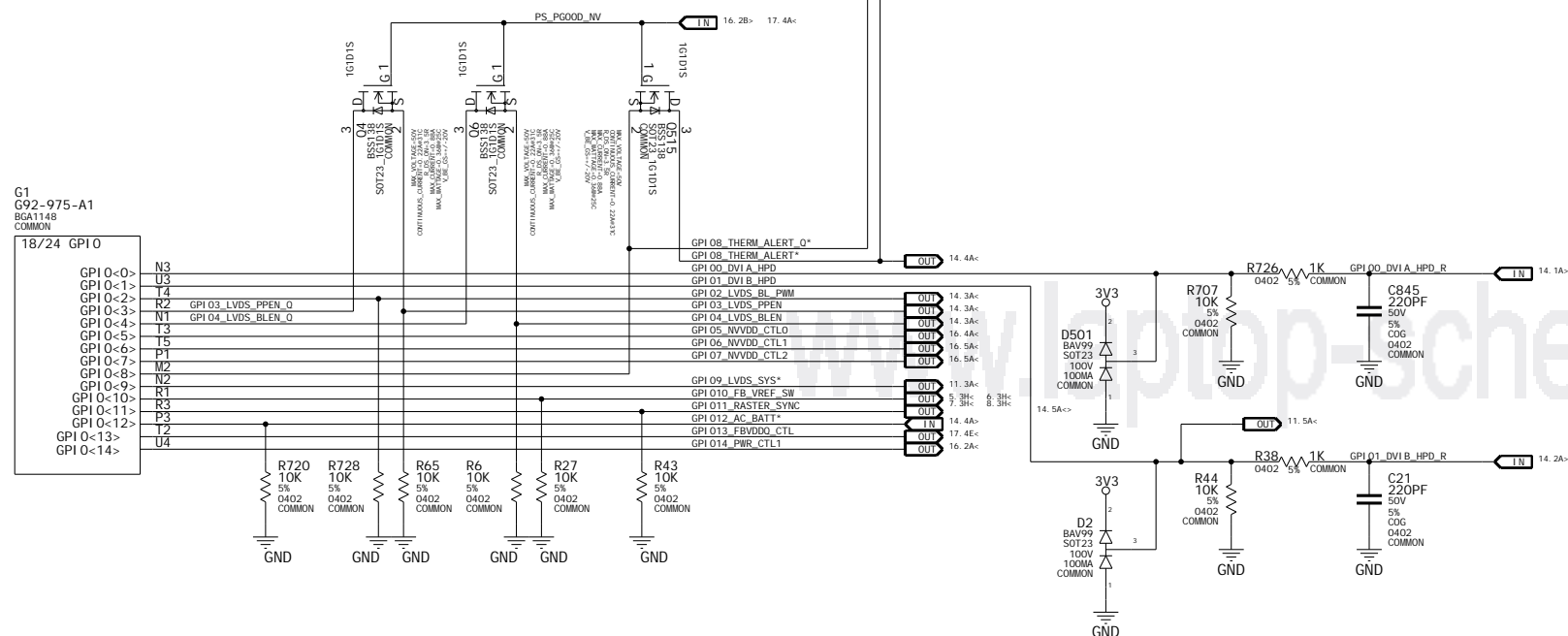
NET		VOLTAGE	MAX_CURRENT	MIN_L1NE_WIDTH
IN	GPU_VID_PLLAVDD	1.2V	0.10A	16MIL
IN	GPU_PLLAVDD	1.2V	0.10A	16MIL
IN	GPU_H_PLLAVDD	1.2V	0.10A	16MIL

NET		NV_IIMPEDANCE	NV_CRTICAL_NET
IN	SPDIF_IN	500HM	1
IN	SPDIF_IN_GPU	500HM	1

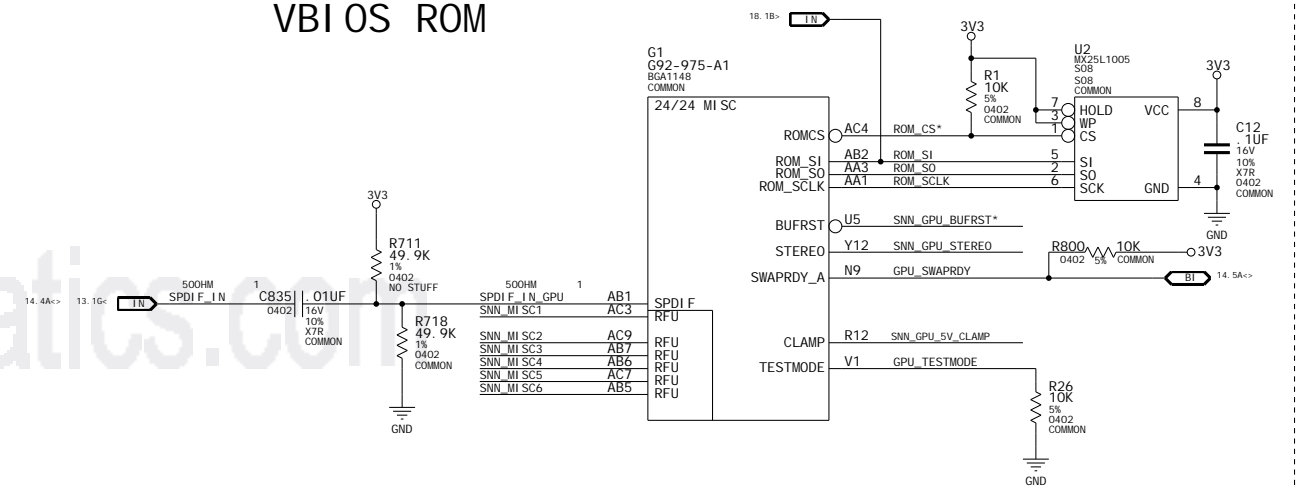
PLLAVDD



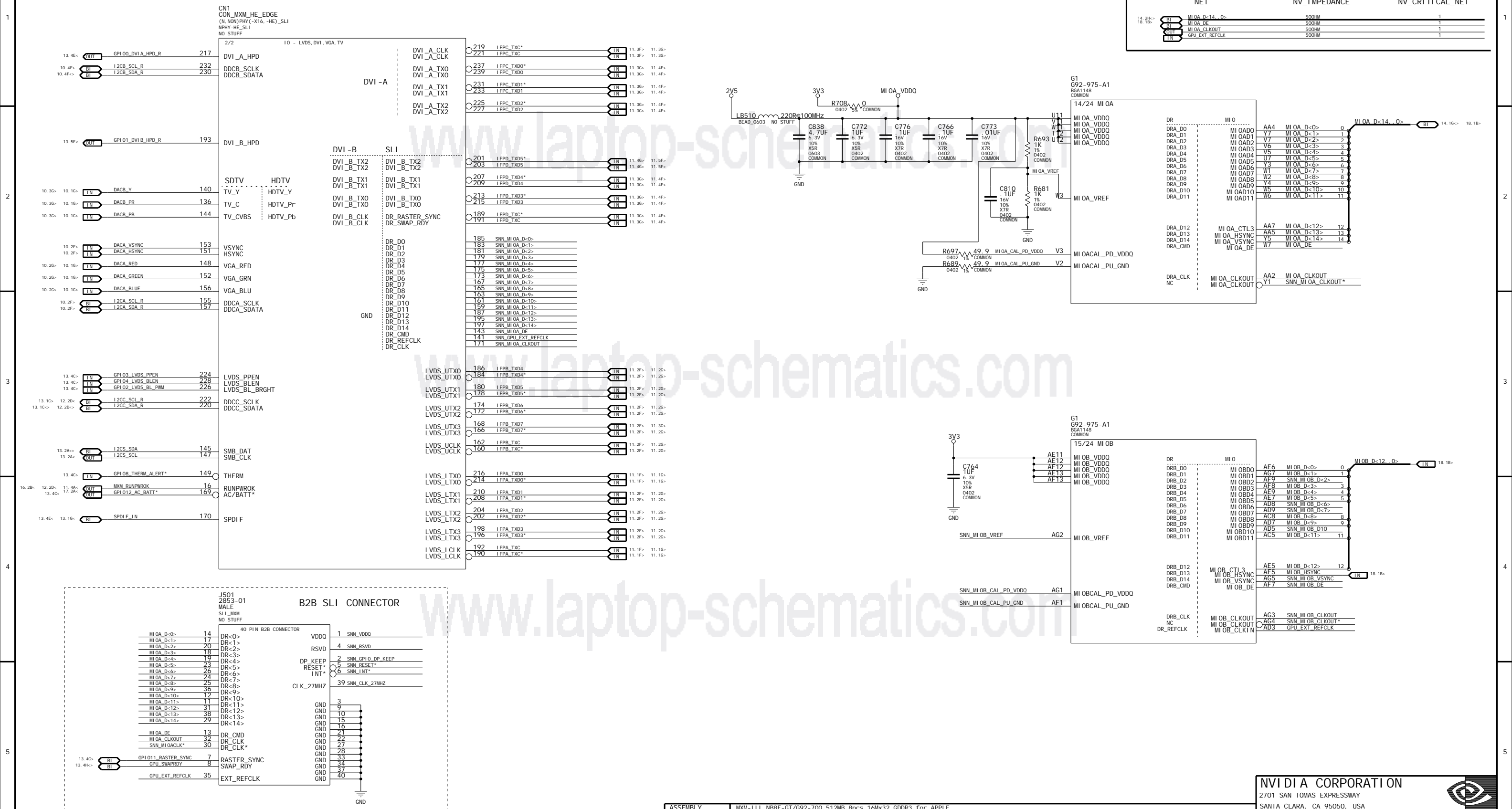
GPI 0

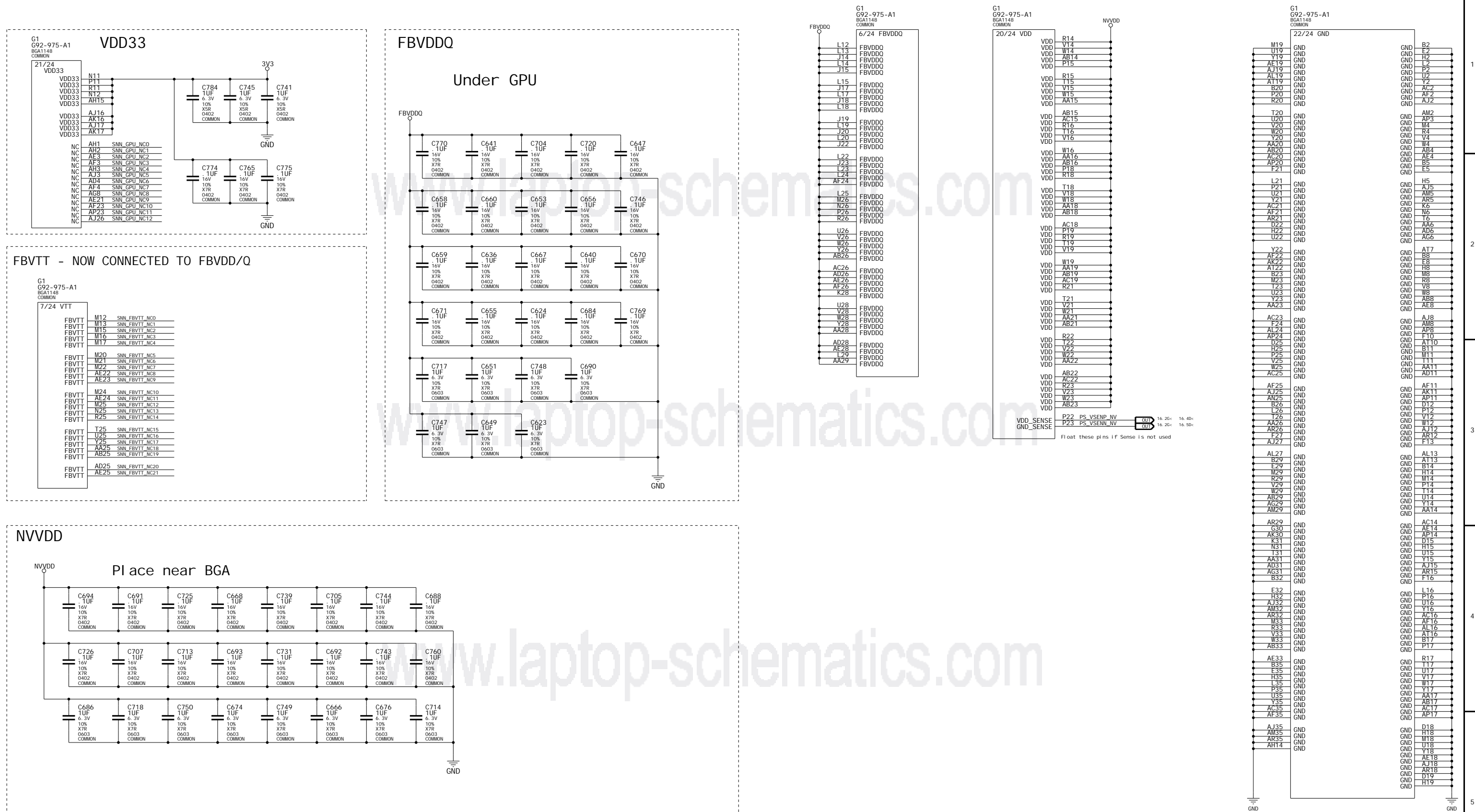


VBI OS ROM



Page14: MXM-III Connector, MI 0A and MI 0B Interface





Page16: Power Supply I - NVVDD

LOAD STEP CIRCUITRY

1

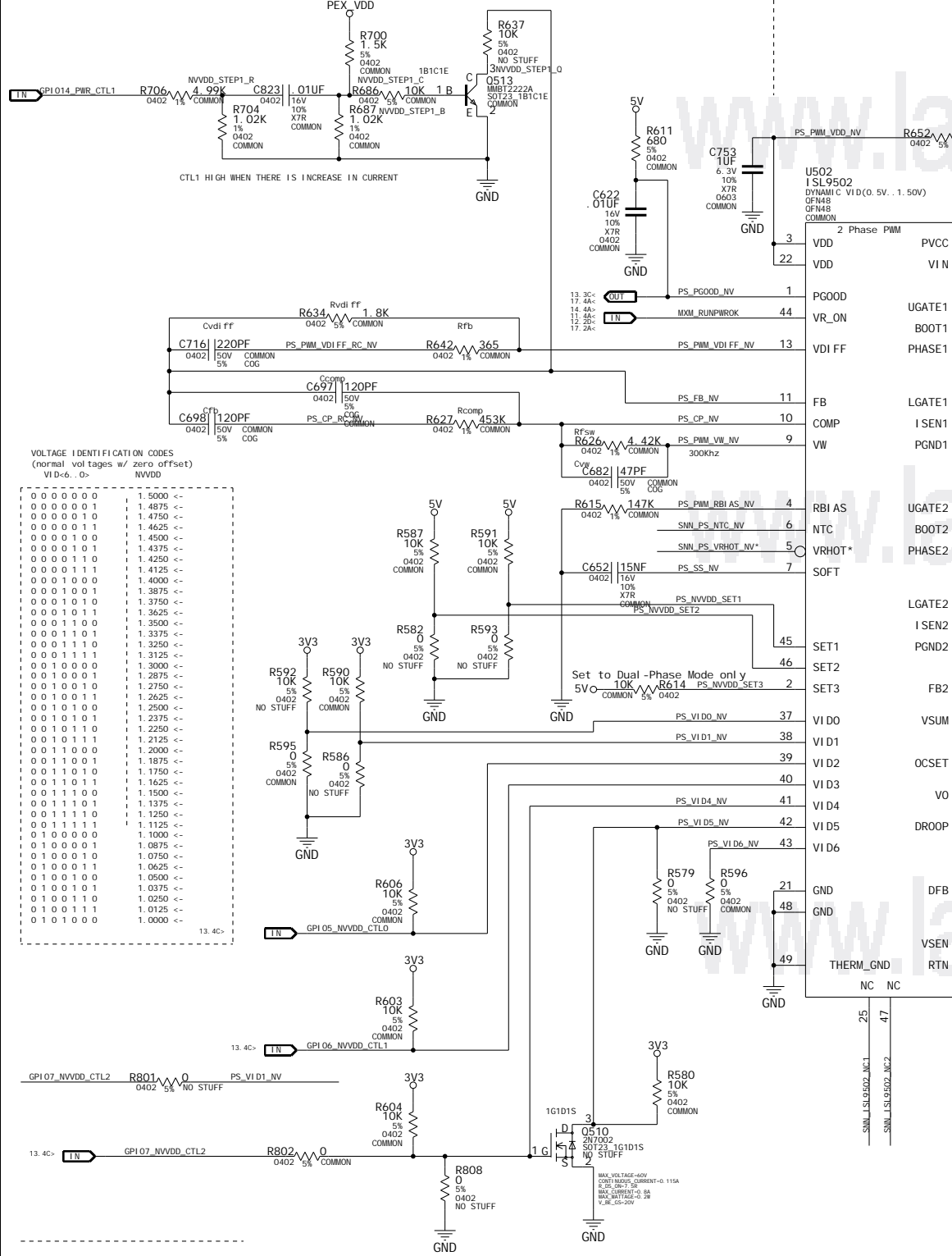
13.35<

2

3

4

5



VOLTAGE IDENTIFICATION CODES
(normal voltages w/ zero offset)
VID<6, 0> NVVDD

0 0 0 0 0 0	1.5000 <-
0 0 0 0 0 1	1.4875 <-
0 0 0 0 1 0	1.4750 <-
0 0 0 0 1 1	1.4625 <-
0 0 0 1 0 0	1.4500 <-
0 0 0 1 0 1	1.4375 <-
0 0 0 1 1 0	1.4250 <-
0 0 0 1 1 1	1.4125 <-
0 0 1 0 0 0	1.4000 <-
0 0 1 0 0 1	1.3875 <-
0 0 1 0 1 0	1.3750 <-
0 0 1 0 1 1	1.3625 <-
0 0 1 1 0 0	1.3500 <-
0 0 1 1 0 1	1.3375 <-
0 0 1 1 1 0	1.3250 <-
0 0 1 1 1 1	1.3125 <-
0 1 0 0 0 0	1.3000 <-
0 1 0 0 0 1	1.2875 <-
0 1 0 0 1 0	1.2750 <-
0 1 0 0 1 1	1.2625 <-
0 1 0 1 0 0	1.2500 <-
0 1 0 1 0 1	1.2375 <-
0 1 0 1 1 0	1.2250 <-
0 1 0 1 1 1	1.2125 <-
0 1 1 0 0 0	1.2000 <-
0 1 1 0 0 1	1.1875 <-
0 1 1 0 1 0	1.1750 <-
0 1 1 0 1 1	1.1625 <-
0 1 1 1 0 0	1.1500 <-
0 1 1 1 0 1	1.1375 <-
0 1 1 1 1 0	1.1250 <-
0 1 1 1 1 1	1.1125 <-
1 0 0 0 0 0	1.1000 <-
1 0 0 0 0 1	1.0875 <-
1 0 0 0 1 0	1.0750 <-
1 0 0 0 1 1	1.0625 <-
1 0 0 1 0 0	1.0500 <-
1 0 0 1 0 1	1.0375 <-
1 0 0 1 1 0	1.0250 <-
1 0 0 1 1 1	1.0125 <-
1 0 1 0 0 0	1.0000 <-

NET	VOLTAGE	CURRENT	LINE WIDTH
NVVDD	1.20V	40A	20MIL
PS_PHASE1_NV		20A	
PS_PHASE2_NV		20A	
PS_VIN_NV			20MIL
PS_U61_NV			20MIL
PS_BOOT1_NV			20MIL
PS_BOOT1_RC_NV			20MIL
PS_LG1_NV			20MIL
PS_ISEN1_NV			16MIL
PS_RC1_NV			25MIL
PS_U62_NV			20MIL
PS_BOOT2_NV			20MIL
PS_BOOT2_RC_NV			20MIL
PS_LG2_NV			20MIL
PS_ISEN2_NV			20MIL
PS_RC2_NV			20MIL
PS_PWM_VSUM_NV			16MIL
PS_PWM_OCSET_NV			16MIL
PS_DROOP_NV			16MIL
PS_PWM_VDI_NV			16MIL
PS_PWM_VDI_FF_NV			16MIL
PS_PWM_VDI_FF_RC_NV			16MIL
PS_FB_NV			16MIL
PS_CP_NV			16MIL
PS_CP_RC_NV			16MIL
PS_PWM_VBIAS_NV			16MIL
PS_SS_NV			16MIL
PS_VSEN_NV			8MIL
PS_VSENN_NV			8MIL

Iout_peak_to_peak = 2.5A
(Iout_max=50A; Vin=7.5V; Vout=1.2V; F=300KHz)

Iout_peak_to_peak = 2.3A
(Iout_max=50A; Vin=7.5V; Vout=1.0V; F=300KHz)

Iin_rms = 10A
(Iout_max=50A; Vin=7.5V; Vout=1.2V)

Iin_rms = 6.3A
(Iout_max=50A; Vin=22V; Vout=1.0V)

	Single-Phase	Dual-Phase
Rvdi ff	1.8K	1.8K
Cvdi ff	150pF	300pF
Rfb	365ohm	365ohm
Cfb	82pF	120pF
Rcomp	732K	412K
Ccomp	100pF	330pF

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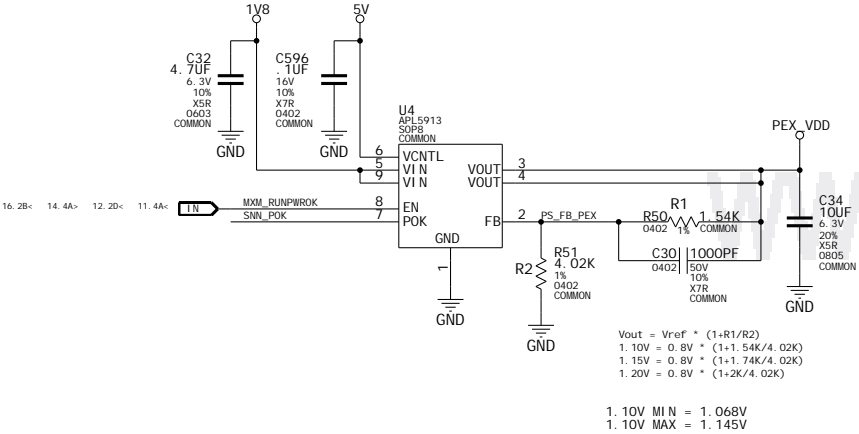
DATE

14-SEP-2007

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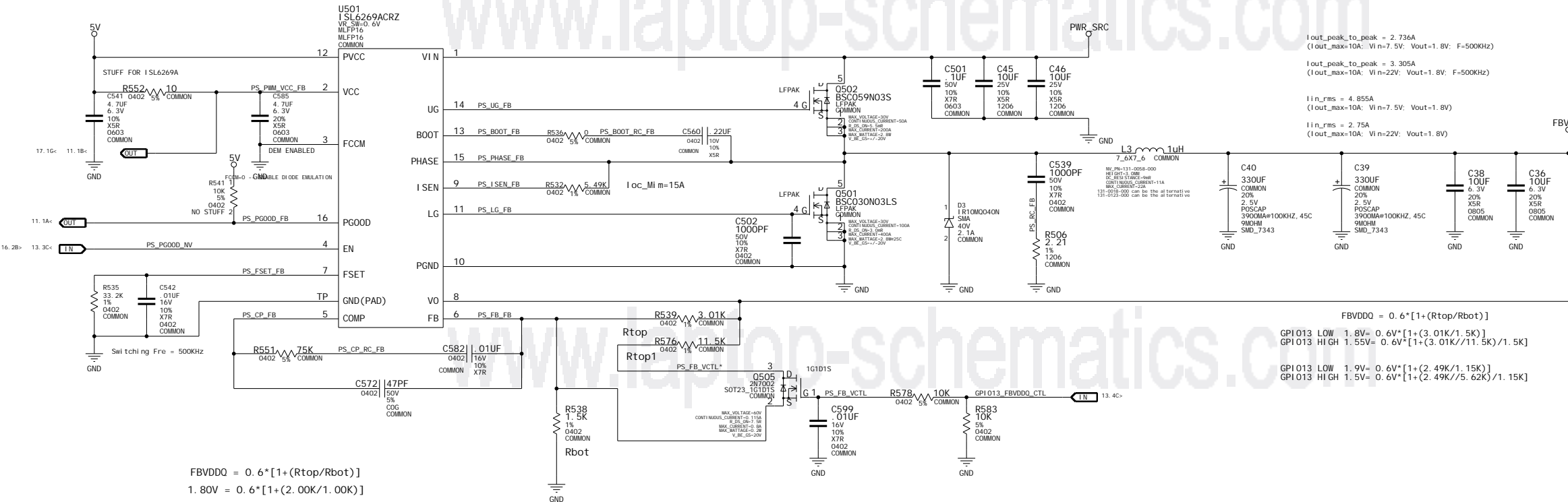
PEX_VDD

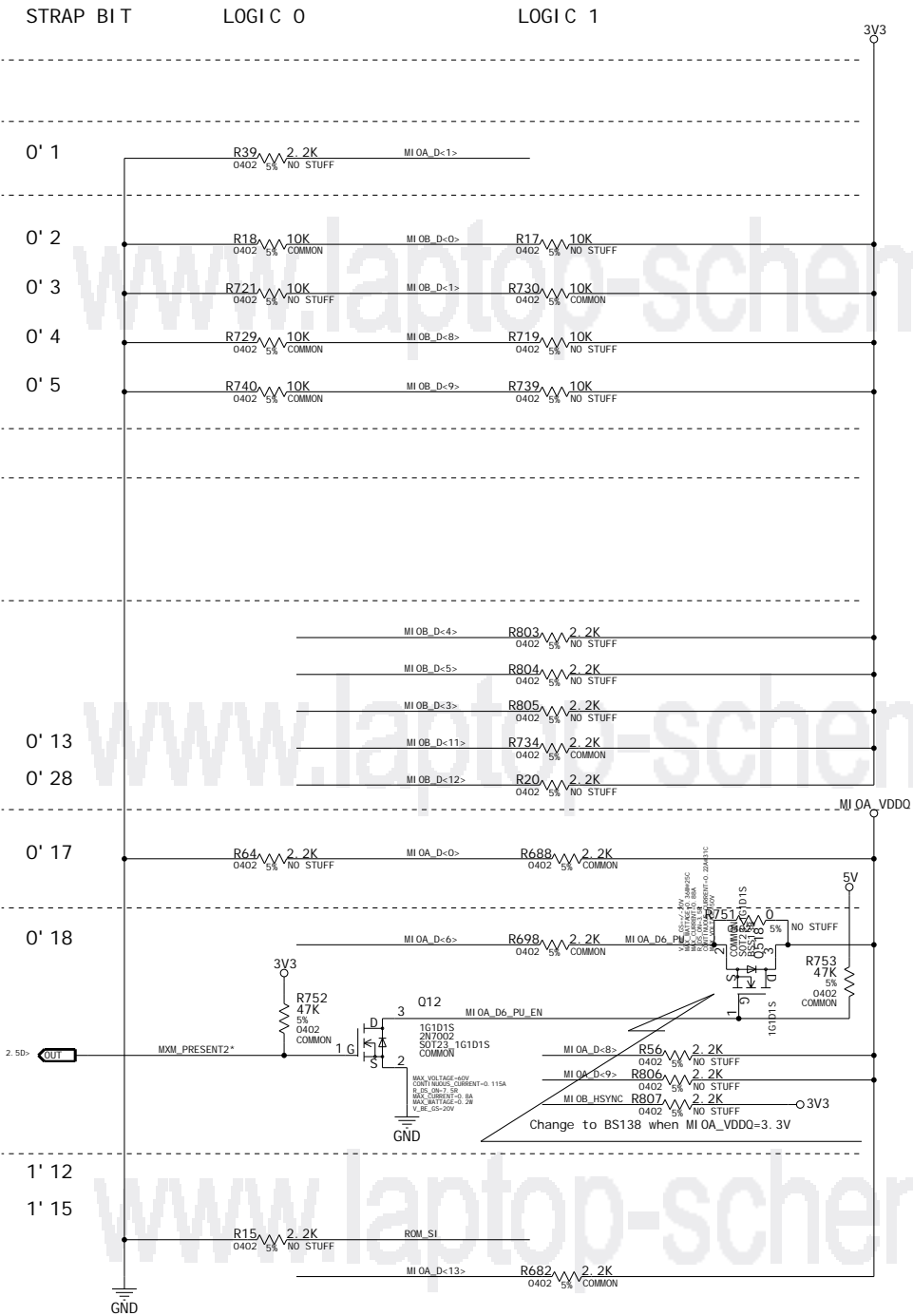
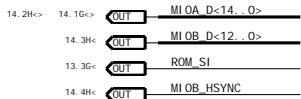
PEXVDD = 1.1V @ 2.25A



NET	VOLTAGE	CURRENT	LINE_WIDTH
FBVDDQ	FBVDDQ	1.8V	10A
PEX_VDD	PEX_VDD	1.2V	2.0A
PS_FB_PEX			16MIL
PS_PHASE_FB		13A	20MIL
PS_PIM_VCC_FB			20MIL
PS_UC_FB			20MIL
PS_LG_FB			20MIL
PS_BOOT_FB			20MIL
PS_BOOT_RC_FB			20MIL
PS_FB_VCTL*			20MIL
PS_CP_FB			16MIL
PS_ISEN_FB			16MIL
PS_FB_FB			16MIL
PS_CP_RC_FB			16MIL
PS_FSET_FB			16MIL
PS_RC_FB			25MIL

FBVDDQ





REG: NV_STRAP_0

PCI_AD_SWAP	0: REVERSED	
	1: NORMAL	DEFAULT
SUB_VENDOR	0: SYSTEM BIOS	
	1: ADAPTER BIOS	DEFAULT
RAM_CFG_0	RAM_CFG[3:0]	
	MS_0001: 16Mx32 DDR3 256-bit Qimonda	
	MS_0010: 16Mx32 DDR3 256-bit Hynix	
	MS_0011: 16Mx32 DDR3 256-bit Samsung	
RAM_CFG_1	MS_0101: 32Mx32 DDR3-Stacked Die 256-bit Qimonda	
	MS_0110: 32Mx32 DDR3-Stacked Die 256-bit Hynix	
	MS_0111: 32Mx32 DDR3-Stacked Die 256-bit Samsung	
RAM_CFG_2	MS_0001: 32Mx32 DDR3-Monolithic 256-bit Qimonda	
	MS_0010: 32Mx32 DDR3-Monolithic 256-bit Hynix	
	MS_0011: 32Mx32 DDR3-Monolithic 256-bit Samsung	
RAM_CFG_3		
CRYSTAL	0: 27MHz	DEFAULT
	1: 14.318MHz	
TV_MODE_0	000: NTSC_M	
	001: NTSC_J	DEFAULT
TV_MODE_1	010: PAL_M	
	011: PAL_N	
	100: PAL_CN	
TV_MODE_2	101: PAL_BDCHI	
	110: RESERVED_0	
	111: RESERVED_1	

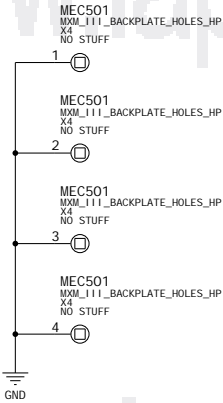
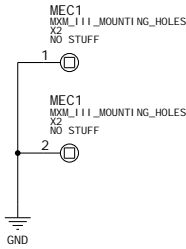
PCI_DEVID_0	DEFAULT: 00000
PCI_DEVID_1	
PCI_DEVID_2	
PCI_DEVID_3	
PCI_DEVID_EXT	

PEX_PLL_EN_TERM100 Per G92 Guide (PEX term)..
* Strap definition inverted
-set to 0x1 to enable
-set to 0x0 to disable

3GIO_PADCFG_LUT_ADR[0]	DEFAULT: 0000
3GIO_PADCFG_LUT_ADR[1]	
3GIO_PADCFG_LUT_ADR[2]	
3GIO_PADCFG_LUT_ADR[3]	

REG: NV_STRAP_1

MI OA_EN_33V	1=3.3V (DEFAULT)
SLOT_CLOCK_CONFIGURATION	1=ENABLE (DEFAULT)



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